In the Claims:

Claim 1: (Original) A semiconductor die package comprising:

a package housing for holding at least one semiconductor die, a substrate and at least one semiconductor die or more than one substrate and multiple semiconductor die, the housing including a base having a top surface for supporting the at least one semiconductor die, side surfaces, and a bottom surface having a plurality of posts extending therefrom, the base including a plurality of holes formed therethrough from the bottom surface to the top surface;

a reference voltage plane within the package housing, said plane electrically coupled to a contact that is at least partially exposed externally of the package housing at one of the sides of the base; and

a plurality of package pins retained in the holes and extending from the bottom surface of the base along the posts.

Claim 2: (Original) The semiconductor die package according to claim 1, wherein the reference voltage plane comprises a power plane.

Claim 3: (Original) The semiconductor die package according to claim 2, further comprising a ground plane within the package housing, wherein said ground plane is electrically coupled to a ground plane contact that is at least partially exposed externally of the package housing at one of the sides of the base.

Claim 4: (Original) The semiconductor die package according to claim 1, wherein the reference voltage plane comprises a ground plane.

Claim 5: (Original) The semiconductor die package according to claim 4, wherein the reference voltage plane comprises a power plane, wherein said power plane is electrically coupled to a power plane contact that is at least partially exposed externally of the package housing at one of the sides of the base.

Claim 6: (Original) The semiconductor die package according to claim 4, wherein said ground plane comprises a grid, wherein said package pins extend through the grid.

Claim 7: (Original) The semiconductor die package according to claim 1, wherein the reference plane is electrically coupled to a plurality of contacts that are at least partially exposed externally of the package housing, at least two of the plurality of contact being exposed at different sides of the base.

Claim 8: (Original) A semiconductor die package comprising:

a package housing comprising a base having a top surface for supporting at least one semiconductor die, multiple substrates and multiple semiconductor dies, or a substrate and at least one semiconductor die, the base including a plurality of holes formed therethrough;

a plurality of electrically-conductive pins retained in the holes and extending from the base externally of the package housing; and

a ground plane grid in the base, wherein said electrically-conductive pins are electrically insulated from and pass through the ground plane grid.

Claim 9: (Original) The semiconductor die package according to claim 8, wherein the base of the package housing further comprises a bottom surface opposite the top surface, the bottom surface having a plurality of posts, wherein the electrically-conductive pins extend axially along the posts.

Claim 10: (Original) The semiconductor die package according to claim 8, further comprising a power plane within said package housing at a periphery or potentially distributed throughout and below the ground plane grid.

Claim 11: (Original) The semiconductor die package according to claim 8, further comprising a ground plane contact exposed externally of the package housing at a side surface thereof, wherein the ground plane contact contacts said ground plane grid.

Claim 12: (Original) The semiconductor die package according to claim 8, further comprising multiple ground plane contacts exposed externally of the package housing at a multiple side surfaces thereof, wherein the ground plane contacts contact said ground plane grid.

Claim 13: (Original) The semiconductor die package according to claim 12, wherein said base has a plurality of indentations along its side surfaces, the multiple ground plane contacts located in the plurality of indentations.

Claim 14: (Original) A combination comprising:

a semiconductor die package having (a) a package housing for holding a semiconductor die, the package housing including a base having a top surface for supporting the semiconductor die, side surfaces, and a bottom surface having a plurality of posts extending therefrom, the base including a plurality of holes formed therethrough from the bottom surface to the top surface, (b) a reference voltage plane within the package housing, said plane electrically coupled to a reference voltage contact that is at least partially exposed externally of the package housing at one of the sides of the base, and (c) a plurality of package pins retained in the holes and extending from the bottom surface of the base along the posts, said package pins having a first end adjacent the top surface and a second end; and

a mating socket comprising (a) a socket housing having a top surface and a bottom surface, the top surface having a plurality of sockets, each socket sized to receive a post of the die package, (b) a plurality of socket contact beams having first ends located in the sockets and second ends extending from the bottom surface of the socket housing, and (c) at least one mating pin having a first end extending from the top surface of the socket housing and a second end extending from the bottom surface of the socket

housing, wherein said package housing is capable of mating with the mating socket such that the posts are received in said sockets, the package pins engage the socket contact beams, and the reference voltage contact engages the mating pin.

Claim 15: (Original) The combination according to claim 14, wherein the second ends of the socket contact beams and the mating pins are located in substantially the same plane and are adapted for electrical connection to a substrate.

Claim 16: (Original) The combination according to claim 14, wherein the reference voltage plane comprises a power plane.

Claim 17: (Original) The combination according to claim 14, wherein the reference voltage plane comprises a ground plane.

Claim 18: (Original) The combination according to claim 14, wherein the reference voltage plane comprises a grid and wherein said package pins extend through the grid.

Claim 19: (Original) The combination according to claim 14, wherein the reference plane is electrically coupled to a plurality of contacts that are at least partially exposed externally of the die package housing, at least two of the plurality of contact being exposed at different sides of the base.

Claim 20: (Original) A combination comprising:

a semiconductor die package including (a) a package housing a base having a top surface for supporting at least one semiconductor die, the base including a plurality of holes formed therethrough, (b) a plurality of electrically-conductive package pins retained in the holes and extending from the base externally of the package housing, (c) and a ground plane grid in the base, wherein said electrically-conductive package pins are electrically insulated from and pass through the ground plane grid; and

a mating socket including (a) a socket housing and (b) a plurality of electrically-conductive socket contact beams held in the socket housing, wherein the semiconductor die package and the mating socket connect together such that the package pins engage the socket contact beams to form electrical connections.

Claim 21: (Original) The combination according to claim 20, wherein the base of the package housing further comprises a bottom surface opposite the top surface, the bottom surface having a plurality of posts, wherein the electrically-conductive pins extend axially along the posts.

Claim 22: (Original) The combination according to claim 20, further comprising a power plane within said package housing at a periphery of the ground plane grid.

Claim 23: (Original) The combination according to claim 20, wherein said die package further includes a semiconductor die supported by said base, the semiconductor die electrically connected to the plurality of package pins and the ground plane grid, and a package lid for sealing the semiconductor die in the base.

Claim 24: (Original) The combination according to claim 23, wherein the die package further comprises solder balls for electrically coupling the semiconductor die to the package pins.

Claim 25: (Original) The combination according to claim 23, wherein the die package further comprises a substrate on which the semiconductor die is mounted and solder balls for electrically coupling the substrate to the package pins.

Claim 26: (Original) The combination according to claim 25, wherein the die package further comprising means for electrically coupling the substrate to the semiconductor die.

Claim 27: (Withdrawn) A method for manufacturing a semiconductor die package, comprising:

molding a package base including a plurality of side walls and a floor having a plurality of holes formed therethrough, wherein interior surfaces of the side walls and floor form a cavity sized to hold a semiconductor die and wherein said molding includes molding an electrically conductive frame into the floor, said frame having a plurality of holes formed therein and the holes through the floor register with the holes of said frame; and

inserting electrically-conductive pins into the holes in the floor such that the pins pass into the holes of the frame and extend from an exterior surface of the floor.

Claim 28: (Withdrawn) The method of claim 27, further comprising:

electrically connecting a semiconductor die to the pins and to the frame; and

attaching a lid to the side walls of the base, the lid and the base sealing the semiconductor die therein.

Claim 29: (Withdrawn) The method of claim 28, wherein said step of electrically connecting comprises:

coupling solder balls to the pins and to the frame and coupling the semiconductor die to the solder balls.

Claim 30: (Withdrawn) The method of claim 28, wherein the step of electrically connecting comprises:

coupling solder balls to the pins and to the frame;

placing a substrate over the solder balls;

placing the semiconductor die on the substrate; and

electrically connecting the semiconductor die to the substrate.